Application Examples and Components Selection

Figures 9 and 10 show the schematic layout and typical components required for correct usage of the SCALE-iDriver. In both cases the primary- side supply voltage (V_{VCC}) is connected between VCC – GND and
supported through a blocking ceramic capacitor C1 (100 nF). Input signal logic is 15 V and it is connected to the IN pin through a resistive voltage driver and Schmitt trigger gates. The SO output has 5 V logic and the R_{SO} is selected so that it does not to exceed I_{SO}.

The secondary insulated power supply (V_{TOT}) is connected between VISO and COM. The positive voltage rail (V_{VISO}) is supported through 4.7 µF ceramic capacitors C_{S21} – C_{S22} connected in parallel. The negative voltage rail (V_{VEE}) is similarly supported capacitors C_{S11} – C_{S12}. Depending on the type of semiconductor that is being driven, the gate charge is different. Typically, the V_{VISO} and V_{VEE} blocking capacitors should have a minimum value calculated as 3 µF per every 1 µC of gate charge. A ceramic capacitor C_{GXX} with value of 10 nF is connected to the GH pin.

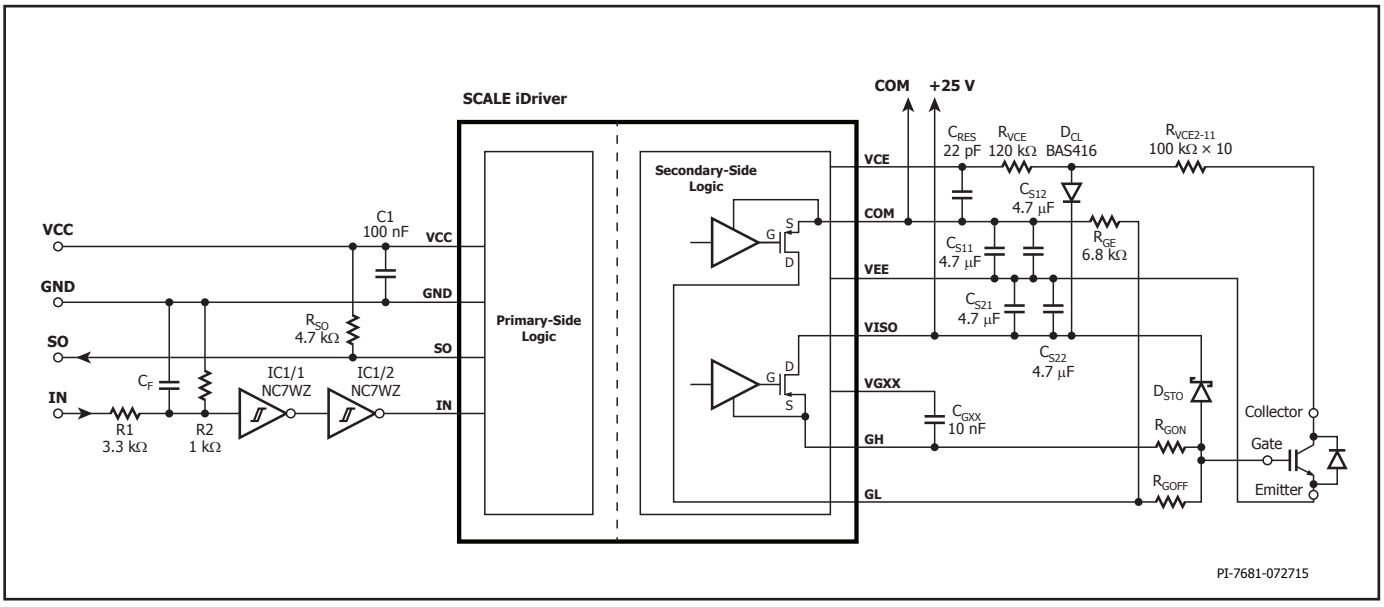

Figure 9. SCALE-iDriver Application Example using a Resistor Chain for Desaturation Detection.

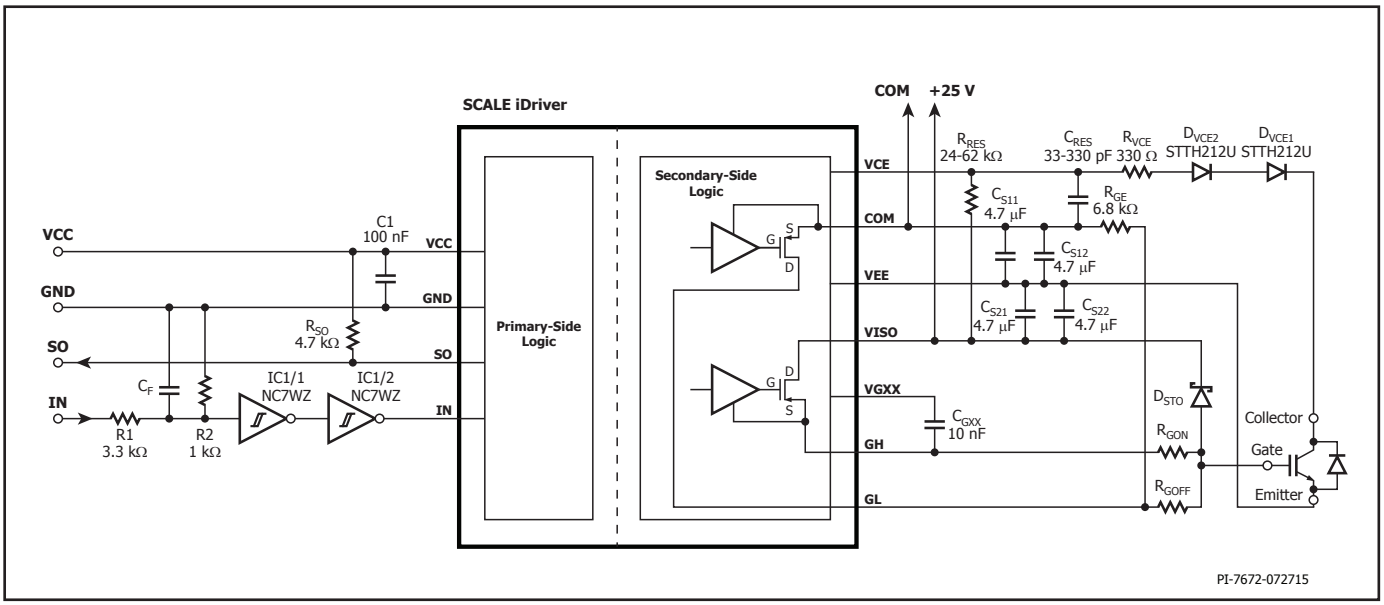

Figure 10. SCALE-iDriver Application Example using Diodes for Desaturation Detection.

The gate of the semiconductor being driven is connected through resistor R_{GON} to the GH pin and R_{GOFF} to the GL pin. If the value of R_{GON} is the same as R_{GOFF} the GH pin can be connected to the GL pin and the gate resistor can beconnected to the gate. In each case, proper consideration needs to be given to the power dissipation and temperature performance of the gate resistor.

To ensure gate voltage stabilization and collector current limitation during a short-circuit, the gate is connected to V_{ISO} through Schottky diode D_{STO} (for example PMEG4010).

To avoid parasitic power switch conduction during system power-on, the gate is connected to COM through 6.8 kΩ resistor.

Figure 9 shows how semiconductor desaturation can be observed using resistors R_{VCE2} – R_{VCE11}. In this example all resistors have a value of 100 kΩ and 1206 size and total value is 1 MΩ. These resistors should be chosen to conduct current between 0.6 mA to 0.8 mA at maximum DC-link voltage. The sum of R_{VCE2} – R_{VCE11} should be approximately 1 MΩ for 1200 V semiconductors and 500 kΩ for 600 V semiconductors. In each case the number of resistors and the package size has to be selected in a way to guarantee at least functional insulation between collector / drain and SCALE-iDriver. The low leakage diode D_{CL} of BAS416 type, keeps the short-circuit duration constant over a wide DC-link voltage range.

Response time is set up through R_{VCE} and C_{RES} (typically 120 kΩ and 22 pF respectively for 1200 V semiconductors). If the short-circuit detection proves to be too sensitive, the C_{RES} value can be increased. The maximum short-circuit duration must be limited to the maximum value given in the semiconductor data sheet.

Figure 10 illustrates the case where semiconductor desaturation is observed using diodes D_{VCE1} and D_{VCE2}. For insulation coordination purposes, two diodes of type STTH212U in a SMB package are used. R_{RES} connected to VISO guarantees current flow through the diodes when the semiconductor is in on-state. When the switch desaturates, the C_{RES} starts to be charged through R_{RES}. In this case the response time is given from the R_{RES} and C_{RES} values. In this application example C_{RES} = 33 pF and R_{RES} = 62 kΩ; if desaturation is too sensitive or the short-circuit duration too long, both C_{RES} and R_{RES} can be adjusted.

Figure 11 shows a recommended PCB layout for the secondary-side (high-voltage) and corresponds to the schematic in Figure 10. The PCB consists of four layers, where top layer makes connection between assembled parts. Layer 2 is connected to the emitter of the IGBT's potential. Layer 3 is connected to V_{ISO} potential and the bottom layer is connected to the potential of COM. It is important to note that layers two, three or the bottom layer must not cover the area below the desaturation diodes D_{VCE1} and D_{VCE2}. This is a critical design issue to avoid coupling capacitance with the SCALE-iDriver's VCE pin and insulation issues within the PCB.

Gate resistors are located physically close to the controlled semiconductor. As these components can get hot, it is recommended that they are placed away from the driver IC.

Short-Pulse Suppression

Command signals applied to the IN pin (pin 7, V_{IN}) are shorter than specified $t_{GE(MIN)}$, so the SCALE-iDriver output signals, GH and GL (pin 13 and pin 16), are extended to value $t_{GE(MIN)}$. The duration of pulses longer than $t_{GE(MIN)}$ will not be changed.

Soft Shut Down (SSD)

This function is activated after a short-circuit is detected. It protects the semiconductor against destruction by limiting the current slope in order to keep momentary V_{CE} below V_{CES} (semiconductor blocking voltage capability). Figure 12 shows the principle of the SSD function. The V_{CE} desaturation is visible during time period P1 (green line) and thanks to rail-to-rail SCALE-iDriver output stage technology, the V_{GE} (gate-emitter voltage, pink line) is kept very stable. After P1 (approximately 5 µs) and according to note 15, V_{GE} is limited to a lower value during a period specified as t_{FSSD}. During t_{FSSD} the short-circuit current slope is limited and initially a small overvoltage V_{CE} occurs. During time period P3, the gate of the semiconductor is being further discharged. Shortly before the discharging process is finished the gate-emitter is connected to $-V_{VEE}$. The remainder of the gate charge is removed, the short-circuit current is switched off and a second small V_{CE} overvoltage occurs. The whole short-circuit current detection and safe switch-off is lower than 10 µs (7 µs in this example).

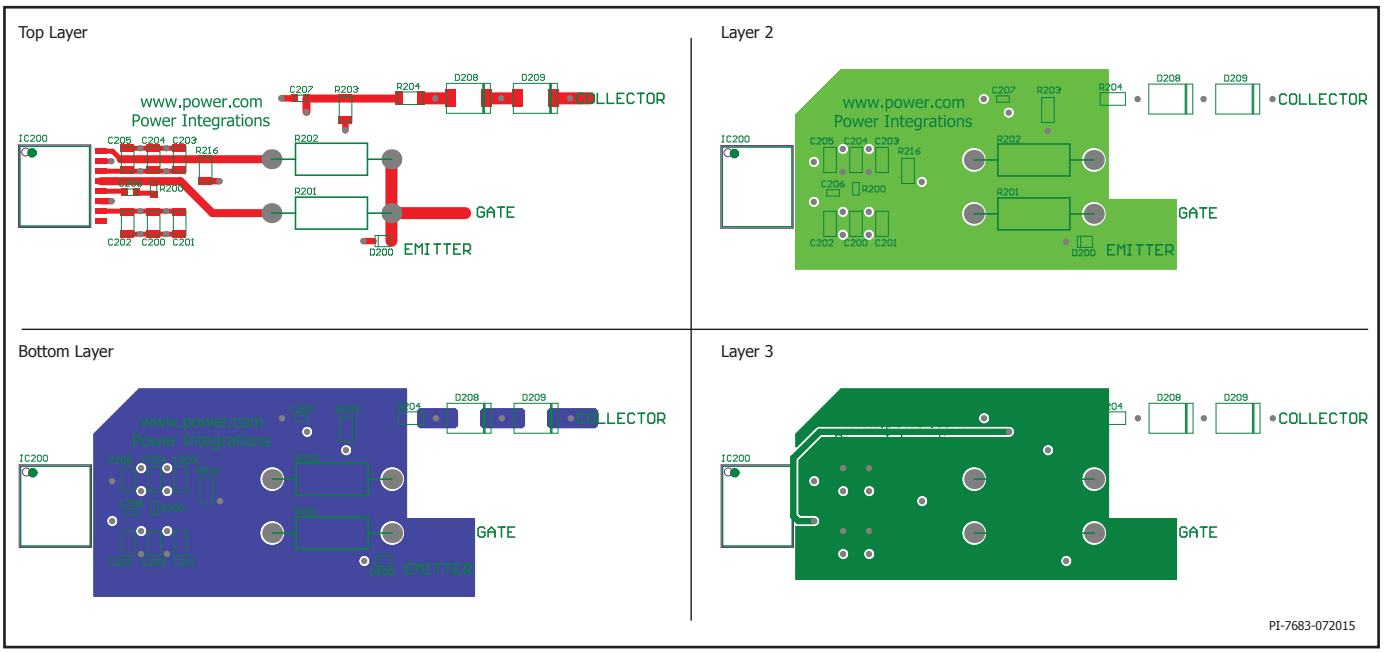

Figure 11. Recommended PCB Layout for Secondary-Side (High-Voltage). Corresponds to Schematic Shown in Figure 10.